SECTION XI

PARALLEL BCD TIME OUTPUT (Option)

SECTION XI-I - GENERAL INFORMATION

DATED: 8-94

1-1 INTRODUCTION

1-2 When installed in a synchronized clock, the Parallel BCD Time Output Option provides an interface to synchronize other equipment. There are two versions of this option. The outputs of the first consists of 42 lines of BCD data from 100's of days to units of milliseconds, four time quality lines to indicate an estimate of the worst-case timing error and two (2) data valid strobe pulses. The second version provides 12 additional lines of BCD data from 100's of microseconds through units of microseconds and an additional data valid strobe.

1-3 PARALLEL BCD OPTION SPECIFICATIONS

OUTPUTS:	Millisecond version: Milliseconds through day-of-year, time quality flags, 1PPS strobe and 1KPPS strobe. Microsecond version: Microseconds through day-of-year, time quality flags, 1 PPS strobe, 1 KPPS strobe and 1 MPPS strobe.
OUTPUT DRIVE:	All data lines are driven by +5 vdc logic capable of driving 15 LSTTL loads or multiple CMOS loads.
LOGIC:	All output lines are "positive true logic".
ACCURACY:	See timing accuracy specification for receiver in section I and data strobe pulse information below.
RESOLUTION:	1 ms or 1 us depending on version.
1 PPS STROBE:	Driven by a 74HCT245 I.C., this line goes to the high state on the second $+90\pm10$ ns and remains high for 500 ms.
1 KPPS STROBE:	Driven by a 74HCT245 I.C., this line goes high on the millisecond + 90 ± 10 ns and remains high for 500 us.

1 MPPS STROBE:	Driven by a 74HCT245 I.C., this line goes high on the microsecond + 90±10 ns and remains high for 500 ns.
CONNECTORS:	Millisecond Version: Rear-panel-mounted female 50-pin D connector. A mating 50-pin male solder-cup D connector is supplied. Microsecond Version: Additional rear-panel-mounted female 25-pin D connector. A mating 25-pin male solder-cup D connector is supplied.
PIN ASSIGNMENT:	See Tables 11-1 and 11-2.

TABLE 11-1
MILLISECONDS CONNECTOR PIN ASSIGNMENT

PIN#	OUTPUT DATA	PIN#	OUTPUT DATA
(1)	GROUND	(26)	10's of min
(2)	NOT USED	(27)	8's of min
(3)	200's of days	(28)	4's of min
(4)	100's of days	(29)	2's of min
(5)	80's of days	(30)	1's of min
(6)	40's of days	(31)	40's of sec
(7)	20's of days	(32)	20's of sec
(8)	10's of days	(33)	10's of sec
(9)	1 KPPS STROBE	(34)	8's of sec
(10)	8's of days	(35)	4's of sec
(11)	4's of days	(36)	2's of sec
(12)	2's of days	(37)	1's of sec
(13)	1's of days	(38)	800's of ms
(14)	TIME QUALITY BIT 2	(39)	400's of ms
(15)	TIME QUALITY BIT 3	(40)	200's of ms
(16)	1 PPS STROBE	(41)	100's of ms
(17)	TIME QUALITY BIT 4	(42)	80's of ms
(18)	20's of hours	(43)	40's of ms
(19)	10's of hours	(44)	20's of ms
(20)	8's of hours	(45)	10's of ms
(21)	4's of hours	(46)	8's of ms
(22)	2's of hours	(47)	4's of ms
(23)	1's of hours	(48)	2's of ms
(24)	40's of min	(49)	1's of ms
(25)	20's of min	(50)	TIME QUALITY BIT 1

( ) Mating solder cup connector pin number

NOTE: When using ribbon cable style mating connectors, the pinout numbering on these connectors may be different.

TABLE 11-2
MICROSECOND CONNECTOR PIN ASSIGNMENT

PIN#	OUTPUT DATA	PIN#	OUTPUT DATA
1	NOT USED	14	GND
2	1'S of us	15	GND
3	2'S of us	16	GND
4	4'S of us	17	GND
5	8'S of us	18	GND
6	10'S of us	19	GND
7	20'S of us	20	GND
8	40'S of us	21	GND
9	80'S of us	22	GND
10	100'S of us	23	GND
11	200'S of us	24	1 MPPS STROBE
12	400'S of us	25	800'S of us
13	NOT USED		

SECTION XI-II - INSTALLATION

2-1 PARALLEL BCD OPTION INSTALLATION

2-2 Supplied with the Milliseconds Parallel BCD Option are the following items:

1) Milliseconds Parallel BCD Interface PCB (Assembly 86-390).
2) Male 50-pin D solder cup mating connector.

Supplied with the Microseconds Parallel BCD Option are the following items:

1) Microseconds Parallel BCD Interface PCB (Assembly 86-390-1).
2) Male 50-pin D solder cup mating connector.
3) Male 25-pin D solder cup mating connector.

2-3 PARALLEL BCD ASSEMBLY INSTALLATION

2-4 **CAUTION:** Disconnect power before installing this assembly. (Failure to do so may result in damage to the assembly). Remove the cover plate from an empty option slot. Slide the Parallel BCD Assembly into the slots on the guide rails and firmly press the card's connector into the mating bus connector. Secure the assembly in the slot with the screws previously removed.

2-5 CABLE FABRICATION

2-6 Use tables 11-1 and 11-2 to fabricate cables. The mating connectors supplied with purchase are a male, 50-pin D connector and a male 25-pin D connector with solder cups (TT P/N 372-50P and 372-25P).

SECTION XI-III - OPERATION

3-1 GENERAL

3-2 Once the user completes the installation and fabricates interface cables, the system is ready for operation. This section describes the operation of the Parallel BCD Output Option.

3-3 OUTPUT DRIVE LEVELS

3-4 All of the data lines are driven by HCTTL parts powered by 5 volts and are capable of driving 15 LSTTL loads or multiple CMOS loads. All data output lines are "positive-true logic".

3-5 TIME QUALITY INDICATORS

3-6 Time quality lines on the 50-pin connector indicate the worst-case time error of the synchronized clock. Refer to SECTION III of this manual under "FUNC 05 - TIME QUALITY ENABLE/SETUP" and "FUNC 14 - EXTERNAL OSCILLATOR FREQUENCY STABILITY". These sections discuss derivation of these indicators and the effect of oscillator-stability selection on the worst-case time error calculation.

3-7 The synchronized clock provides an estimate of the worst-case error based on the user-entered oscillator drift rate. This estimate is indicated by each of the four time quality lines changing to the high state in turn as the worst-case error calculation exceeds the threshold for that line. A linear drift rate at the specified oscillator stability is used to evaluate the estimated worst-case error. An estimate of the worst-case time error may be determined from the table below. The first column shows the pin number of the rear panel 50-pin connector. The second column shows the worst-case error threshold at the transition from low to high on that pin. The error thresholds are set with Function 05.

TABLE 11-2
TIME QUALITY INDICATORS

PIN #	ESTIMATED WORST-CASE ERROR
ALL PINS LOW	Less than First Threshold
(50) GOES HIGH	First Threshold
(14) GOES HIGH	Second Threshold
(15) GOES HIGH	Third Threshold
(17) GOES HIGH	Fourth Threshold

( ) Mating connector pin number

NOTE: Some mating connector pinouts are numbered differently. Use Rear panel Connector pinout numbers.

3-8 When time is again synchronized, the time quality lines will again go low as the unit re-corrects to the proper time. At initial turn-on or after a power failure, the time quality lines will remain in the high state until the clock has synchronized. The time quality lines can, therefore, be used as read-inhibit lines to guarantee a given timing accuracy.

3-9 1 PPS, 1 KPPS AND 1 MPPS STROBE LINES

3-10 Both 1 PPS and 1 KPPS strobe lines on the 50-pin output connector and the 1 MPPS strobe line on the optional 25-pin connector indicate valid BCD time data.

3-11 The 1 PPS 50% duty cycle output line on Pin (16)[6] of the 50-pin connector switches to the high state 90±10ns after the second. This allows the user to use the rising edge of this strobe to clock data into a remote system. The 90 ns nominal delay allows for the output register time delay plus the user's interface setup-time requirements. At any time the 1 PPS strobe line is high, the data lines from seconds up will not be changing states and are therefore available for reading.

3-12 The 1 KPPS 50% duty cycle output line on pin (9)[20] of the 50-pin connector switches to the high state 90±10 ns after the millisecond. The 90 ns nominal delay allows for the output register time delay plus the user's interface set up time requirements. At any time the 1 KPPS line is high, the data lines from milliseconds up will not be changing states and are therefore available for reading.

3-13 The 1 MPPS strobe is available only in the microsecond version of the Parallel BCD Option. The 1 MPPS 50% duty cycle output line on pin #24 of the 25-pin connector switches to the high state 90±10 ns after the microsecond. The 90 ns nominal delay allows for the output register time delay plus the user's interface set up time requirements. At any time the 1 MPPS line is high, the data lines from microseconds up will not be changing states and are therefore available for reading.

SECTION XI-IV - THEORY OF OPERATION

4-1 The 86-390 Assembly outputs parallel BCD data milliseconds through day-of-year as well as time quality data.

4-2 Registers U23, U1, U5, U11, U8, U14, and U19 latch data buffered by transceiver U4 one count ahead of the current time. PAL U7 and 1 of 8 decoder U10 control the appropriate clock pulse to these data latches. Registers U24, U2, are clocked by the on-time edge of the 1KPPS. U6, U12, U9, U15, and U20 are clocked by the on-time edge of the 1 PPS. All data outputs at connector P3.

4-3 Counters U22, U18 and U21 store the microseconds count. The count is reset each millisecond by flip-flop U17:A. The reset pulse width is trimmed to 100 ns by U17:B.

4-4 The 1 PPS, 1 KPPS and 1 MPPS data strobes are delayed to compensate for chip delays and user set-up time. Transceiver U16 buffers 1 PPS, 1 KPPS and 1 MPPS while delay line U13 delays the on-time edge by approximately 70 ns. The delayed signal is again buffered by U16 to connector P3 (introducing an additional delay of approximately 20 ns).

SECTION XI-V - MAINTENANCE AND TROUBLESHOOTING

5-1 TROUBLE SHOOTING

5-2 **CAUTION:** Only a qualified electronics technician should attempt repairs. Exercise caution while working on or near power supply assemblies.

5-3 Since apparent problems may be the result of operator error, the technician will need a thorough understanding of normal operation.

5-4 Before assuming a malfunction, first verify that the system using the output is functioning properly. Second, verify that cables have been properly fabricated and are good. Verify that the assembly is firmly plugged into the bus connector.

5-5 If the Parallel BCD Assembly does not output data, check the +5vdc supply voltages. Use the schematics in this section to trace defective lines to a faulty component.